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Donna M. Colon

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of

Inventor: Laptev, P.

Serial No. 09/829,587

Filed: 04/09/2001

For: SYSTEM FOR, AND METHOD OF, ETCHING A SURFACE ON A WAFER

Confirmation No. 7932

Examiner: Zervigon, R.

Group Art Unit: 1763

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FOURTH SUPPLEMENTAL APPEAL BRIEF

Commissioner for Patents
MAIL STOP APPEAL BRIEF - PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I. Real Party in Interest

Sputtered Films, Inc., the assignee of record of the application.

II. Related Appeals and Interferences

None.

III. Status of Claims

Claims 1-21 and 43-51 have been rejected by the Examiner on the basis of prior art cited by the Examiner. Claims 22-42 have been withdrawn from prosecution in the application. Claims 1-51 have been, and are, the only claims in the application. The rejection of claims 1-21 and 43-51 is being appealed.

IV. Status of Amendment

Applicant filed a proposed amendment under Rule 116 on October 30, 2003 to amend one (1) word in each of claims 1, 3, 8, 48 and 49, so as to make the claims consistent with the disclosure in the specification and the drawings. In an Office Action dated 11/07/2003, the Examiner refused to enter the proposed amendment on the ground that applicant's amendment to claim 3 changing "less" to -- greater -- "requires additional consideration of the cited prior art." Applicant has accordingly written claims 1, 3, 8, 48 and 49 in this Third Supplemental Appeal Brief without including applicant's proposed changes in the claims.

V. Summary of the Claimed Subjected Matter – Specification from page 7, line 3 through page 15, line 17

Figures 1-4 show a preferred embodiment, generally indicated at 10, of apparatus for etching a surface 12 of an insulating layer 14 in a wafer generally indicated at 16. As will be appreciated, the wafer may be formed from a plurality of stacked layers, some of them electrically conductive and others electrically insulating. In addition to the insulating layer 14, an electrically conductive layer 15 and an electrically insulating base layer 17 are schematically shown to represent the different layers in the integrated circuit

chip. The insulating layer 14 may have a plurality of a grooves or sockets 18. The insulating layer 14 may illustratively be made from a suitable material such as a polyamide.

The insulating layer 14 may illustratively have a thickness of approximately three (3) microns. The sockets 18 may be completely, or partially, formed through the thickness of approximately three (3) microns in the insulating layer 14. Figure 2 illustratively shows the sockets 18 as extending completely through the thickness of the insulating layer 14. The preferred apparatus 10 of this invention illustratively may etch approximately one hundred angstroms (100 ÿ) from the surface 12 of the insulating layers 14 in a smooth and even layer and without any pits in the layer.

The apparatus 10 includes an enclosure 20 which may be formed in part by an electrode 22, and electrode 24 displaced from, but preferably substantially parallel to, the electrode 22 and magnets 26 and 28 disposed in a transverse (preferably substantially perpendicular) relationship to the electrodes 22 and 24. The electrode 22 is disposed in a contiguous but spaced and substantially parallel relationship to the wafer 16 and is movable in position toward or away from the wafer, as indicated by a double-headed arrow 25. The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1 – 2mm. A plate 30 extending from the magnet 28 in a substantially parallel and adjacent, but spaced, relationship to the electrode 22 also defines the enclosure 20. A ring 32 extending from the magnet 26 to a position spaced from, but adjacent to, the electrode 24 also defines in part the enclosure 20. The plate 30 and the ring 32 may be considered as electrical conductors.

The magnets 26 and 28 preferably constitute permanent magnets but they may also constitute magnetizable members on which windings are disposed to produce a saturable magnetic flux when a current flows through the windings. The magnets 26 and 28 may have a north polarization (indicated by the letter "N" in Figure 1) at their positions of contiguity and may have a south polarization (indicated by the letter "S" in Figure 1) at their opposite ends. The magnets 26 and 28, the plate 30 and the ring 32 are provided with a reference potential such as a ground 34. The wafer 16 is disposed in close proximity to the electrode 22 within the enclosure 20 and in substantially parallel relationship to the electrode. The wafer 16 is at a floating potential.

The electrode 22 receives a relatively low AC voltage from a power supply 36 at a suitable frequency such as approximately 13.56 MHz. As will be explained in detail subsequently, this causes the electrode 22 to receive a relatively low negative DC bias such as a negative bias in the order of -100 volts to -500 volts. A matching network 38 is preferably disposed electrically between the power supply 36 and the electrode 22 to match the impedance of the power supply to the impedance of the electrode.

The electrode 24 receives a relatively high AC voltage from a power supply 40 at a suitable frequency such as approximately 13.56 MHz. As will be explained in detail subsequently, this causes the electrode 24 to have a relatively high negative DC bias such as a negative bias in the order of -1000 volts to -3000 volts. A matching network and zero bias circuit 42 are preferably disposed electrically between the power supply 40 and the electrode 24 to match the impedance of the power supply to the impedance of the electrode and to provide substantially a ground potential on the

electrode. The zero bias circuit may constitute an inductance between the electrode 24 and ground to provide a high impedance for alternating voltages and to provide a low impedance for a DC voltage. The power supplies 36 and 40 may constitute a single power supply.

A conduit 44 is provided for introducing molecules of an inert gas such as argon into the enclosure 20 from a source 45. The argon molecules pass into the enclosure 30 through the space between the electrode 24 and the ring 32. The argon molecules pass out of the enclosure 20 through the space between the plate 30 and the wafer 16. The argon gas flow through the enclosure 30 may illustratively be at a flow rate of 0.1-50 SCCM at a working pressure of 0.5-5mTorr. The movement of the argon molecules through the enclosure 20 is facilitated by a vacuum pump 47.

A negative bias is produced on the electrode 22 because of the alternating voltage applied to the electrode. In the positive half cycles of the alternating voltage, the electrode 22 attracts electrons because of the electrical field between the electrode and the ground potential 34 on the plate 30. In the negative half cycles of the alternating voltage, positive ions are attracted to the electrode because of the electrical field between the electrode and the ground potential 34 on the plate 30. Since the electrons are considerably lighter in weight than the positive ions, they move faster toward the electrode 22 than the positive ions. This causes the electrons to accumulate in the space adjacent the electrode 22, thereby producing the negative DC bias on the electrode. The electrode 24 receives a negative bias because of the same physical phenomenon. However, the negative bias on the electrode 22 is considerably less than the negative DC

bias on the electrode 24 because of the differences in the voltages applied to the electrodes.

As previously indicated, the magnetic field produced by the magnets 26 and 28 is substantially perpendicular to the electrical fields produced by the electrodes 22 and 24. This causes electrons in the enclosure 20 to move in a spiral or helical path between the electrode 22 and the plate 30, and between the electrode 24 and the ring 32, because of the ground potentials on the plate and the ring. The electrons strike molecules of argon gas and ionize these molecules. Since the electrical field between the electrode 24 and the ring 32 is considerably stronger than the electrical field between the electrode 22 and the plate 30, most of the ionization of argon molecules occurs in the region of the electrode 24. Some of these argon ions then move into the region of the electrode 22.

Figure 3 illustrates at 46 lines of force produced by the electrical field between the electrode 22 and the plate 30. Arrows indicate the direction of the lines 46 of force. The electrons in the enclosure 20 travel in a spiral or helical path along the force lines 46, the spiral or helical path resulting from the force of the magnetic field as the electrons move along the force lines 46. In like manner, Figure 3 illustrates at 48 lines of force produced by the electrical field between the electrode 24 and the ring 32 and between the electrode and the grounded magnets 26 and 28. The electrons in the enclosure 20 travel in a spiral or helical path along the force lines 48 because of the force on the electrons by the magnets 26 and 28.

Applicant's assignee of record in this application has previously sold one (1) unit of apparatus with features similar to the apparatus shown in Figure 1. This unit

may have been sold more than one (1) year prior to the date of this application. However, there is one significant difference between the apparatus 10 constituting the preferred embodiment of the invention and the unit previously sold by applicant's assignee. The significant difference is that the wafer 16 engaged the electrode 22 in the one (1) unit sold prior to the date of this application. The circuit equivalent of this arrangement is shown in Figure 5b and is indicated as prior art in that Figure. As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention.

As will be seen, the combination of the electrode 22 and the wafer 16 in Figure 5a is seen as a single electrode or plate in a capacitor 50 in Figure 5b. The other electrode or plate in the capacitor 50 is defined by the positive ions in the enclosure 20 at positions adjacent the electrode 24. These positive ions are schematically illustrated by dots (.) at 51 in Figure 3. The dielectric between the plates of the capacitor 50 may be considered to be the insulating layer 14. The impedance of the capacitor 50 is accordingly relatively low because the insulting layer 14 is relatively thin and because the dielectric constant of the insulating layer is lower than the dielectric constant of air or the dielectric constant of a vacuum.

Since the impedance of the capacitor 50 is relatively low, a relatively large current flows through the capacitor. This current results from the attraction of the argon ions to the insulating layer 14 because of the negative DC voltage on the electrode 22. The relatively large current produces an etching of molecules and ions from the surface 12 of the insulating layer 14. This etching is of such a force that the etching is not

smooth, even or uniform. Pitting of the surface of the insulating layer 14 accordingly occurs. The problem is particularly aggravated in considering the etching of the walls of the sockets 18 in the insulating layer 14.

Since the etching does not result in a smooth, even and uniform surface 12 of the insulating layer 14, any subsequent deposition of an electrically conductive layer on the surface 12 has significant differences in thickness of the electrically conductive material at different positions on the surface 12. This significantly affects the electrical characteristics of the electrical deposition on the insulating layer 14 and produces significant deterioration in the performance characteristics of the integrated circuit chips formed from the wafer.

As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention. The separation may be in the order of 0.1 to 2.0 millimeters. This causes two (2) capacitors 52 and 54 in Figure 4b to be defined by the electrode 22, the wafer 16 and the charge produced by the argon ions 51 in the enclosure 20 in the vicinity of the electrode 22. The plates of the capacitor 52 in Figure 4b may be respectively considered to be defined by the electrode 22 and by the electrically conductive deposition layers in the wafer 16. Although there may be argon ions in this gap, the argon ions are relatively small in number. Furthermore, the gap is so small that the argon ions cannot be accelerated to any significant degree. Because of these factors, the dielectric in the capacitor 52 in Figure 4b may be considered to be the gap between the electrode 22 and the wafer 16. This gap causes the impedance of the capacitor 52 to be relatively high. This impedance can be adjusted to any desired value

by adjusting the position of the electrode 22 in the opposite directions 25 to vary the distance between the electrode and the wafer 16.

The capacitors 52 and 54 may be considered to be in series as shown in Figure 4b. The capacitor 54 may be considered to have plates defined by the electrically conductive layers in the wafer 16 and by the charge provided by the argon ions 51 in the enclosure 20 in the vicinity of the electrode 22. The dielectric for the capacitor 54 may be considered to be the insulating layer 14. The impedance of the capacitor 54 is relatively low, particularly in relation to the impedance of the capacitor 52, because of the thin dimension of the insulating layer 14 and the dielectric constant of the insulating layer.

The current through the series circuit including the capacitors 52 and 54 in Figure 4b is limited and controlled by the capacitor 52 because of the high impedance of the capacitor. This limited and controlled current provides a gentle etching of the surface 12 of the insulating layer 14 and of the walls of the sockets 18. As a result, any specified amount of material may be etched from the surface 12 of the insulating layer 14 and from the walls of the sockets 18. For example, an etching of the material of the insulating layers 14 and the walls of the sockets 18 may be provided in a thickness of approximately one hundred ÿngstroms (100 ÿ).

The etching produces smooth, even and uniform surfaces of the insulating layer 14 by the apparatus 10 as a result of the etching. This provides for a deposition of a smooth, uniform and even thickness of an electrically conductive material on the etched surface of the insulating layer 14. The etching of the walls in the sockets 18 is also even,

uniform and smooth. This constitutes a distinct advance over the prior art, even the prior art as represented by the single unit of the apparatus sold by applicant's assignee prior to the filing date of this application, this prior unit being shown in Figure 5a and being represented by the electrical circuitry shown in Figure 5b.

As shown schematically in Figure 4a, the balls 60 made from a suitable material such as copper may be provided on the electrically conductive surface of the wafer 160. The balls 60 operate as electrical leads. The balls 60 are known in wafers of the prior art. The balls 60 are not affected by the actions of the capacitances 52 and 54 in Figure 4b.

V(a). Insert on page 15, lines 14-17 to specification

In the Office Action dated 03/09/2004, the Examiner has made the following request:

> "The Summary of the invention leaves out the most important part of the invention stated on page 15, last paragraph. As a result, the brief does not contain a concise statement of the issues presented for review as required by 37 CFR 1.192 (c)(6)."

In view of this strong and urgent statement by the Examiner, applicant has added the portion of the specimen on page 15, lines 14-17. This portion of the specification reads as follows:

> "As shown schematically in Figure 4a, balls 60 made from a suitable material such as copper may be provided on the electrically conductive surface of the wafer 160. The balls 60 operate as electrical leads. The balls 60 operate as electrical leads. The balls 60 are not affected by the actions of the capacitances 52 and 54 in Figure 4b."

Applicant notes that the numeral "160" on page 15, line 15 should be changed to – 16 --. Applicant will make this change after the Board's decision and the return of the application to the Examiner for further prosecution.

Applicant will be interested in learning from the Examiner in the Examiner's answer how the paragraph on page 15, lines 14-17 of the specification constitutes "the most important part of the invention." Applicant notes that the Examiner has not discussed this paragraph in relation to any of applicant's claims in any of the Office Actions of the Examiner and has not applied this paragraph against any of applicant's claims in any of the Office Actions of the Examiner.

VI. Grounds of Rejection to be Reviewed on Appeal

The Examiner has provided two (2) grounds of rejection as follows:

A. Rejection of Claims as Anticipated by Koshimizu as Demonstrated by Mountsier patent 5,810,933/.

1. Claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 51. These claims have been rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu patent 5,980,687 as demonstrated by Mountsier patent 5,810,933.

B. Rejection of Claims as Being Unpatentable Over Koshimizu in view of Mountsier.

Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51. These claims have been rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu patent 5,980,687 in view of Mountsier patent 5,810,933.

Applicant respectfully submits that the Examiner's grounds of rejection (6)(A) and (6)(B) are imprecise and actually, hopefully without offending the Examiner, they are improper. They fail to recognize the considerable differences between the combinations recited in the claims in each of 6(A) and 6(B) and also the interrelationship between claims in each of the grounds of rejection. For example, applicant has included claims 2, 5, 6, 9, 16, 45, 46, 47 and 50 in a first ground of rejection as specified subcomponents. From the claims in applicant's proposed first ground of rejection, claims 2, 16, 46 and 47 have been classified by the Examiner in ground 6(A) and claims 5, 6, 7 and 50 have been classified by the Examiner in ground 6(B). This indicates that, in applicant's opinion, the Examiner's grounds of rejection are improper.

Applicant is concerned that the Examiner's improper rejection of claims in grounds 6(A) and 6(B) may prevent applicant from obtaining the allowance of claims that should actually be allowed. For example, all of the claims in ground 6(A) may be rejected on the basis of the rejection of one (1) claim in ground 6(A). The rejected claim may not properly belong in the ground 6(A) of rejection.

As another example, applicant has listed claims 11, 14, 19, 48, 49 and 50 in another proposed ground of rejection of the claims. In this ground of rejection, claims 11, 14, 19 and 51 have been listed by the Examiner in the ground 6(A) of rejection and claims 48 and 49 have been listed by the Examiner in the ground 6(B) of rejection. This constitutes another example where the Examiner has listed, in two (2) separate grounds of rejection, claims which, in applicant's opinion, should have been listed in the same ground of rejection.

As will be seen from the above discussion, applicant respectfully submits that claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 51 in the Examiner's ground 6(A) of rejection do not stand or fall together and that claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 in the Examiner's second ground of rejection do not stand or fall together. Applicant respectfully disagrees with the grounds of rejection by the Examiner. As will be seen from the subsequent discussion, there is a considerable distinction between what is being claimed in each of the individual claims constituting the Examiner's ground 6(A) of rejection and there is also a considerable distinction between what is being claimed in each of the individual claims constituting the Examiner's ground 6(B) of rejection. There is also no commonality of the grounds of rejection among claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 51 in the Examiner's ground 6(A) of rejection and no commonality among claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 in the Examiner's ground 6(B) of rejection.

The Examiner has indicated that applicant has not provided a concise statement of the issues and implies that the Examiner has provided a concise statement of the issues. For example, the Examiner implies that the following constitutes a concise statement of the issues.

> "For example, should the rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43, 44, 45, 46, 47 and 50 under 15 U.S.C. 102 as being anticipated by Koshimizu (U.S. patent 5,810,687) and demonstrated by Mountsier et al. (U.S. patent 5,810,687) be sustained?"

Applicant will concede that the Examiner's language is concise. The problem is that there is no commonality of what is recited in claims 1, 4, 7-9, 11, 12, 14-16, 19-21, 43-47 and 50. Since there is no commonality of what is recited in these claims, the Board of Appeals could reject one of the claims in this ground of rejection. A rejection of one of the claims in this ground may mean that all of the other claims in this ground are rejected even though these other claims recite combinations of elements completely different from the combination of elements in the rejected claim. By grouping the claims on the basis of commonality of subject matter in the claims, applicant avoids the possibility that all of the claims in an enlarged group of unrelated claims will be rejected merely because one of the unrelated claims in the group is rejected.

Applicant proposes the following grounds of rejection of the claims and indicates below, for each ground, how the claims in that ground are patentably distinguished from the claims in the other grounds and from Koshimizu as demonstrated by Mountsier and from Koshimizu in view of Mountsier. Applicant also indicates how each of the claims in each group is distinguished patentably from the other claims in the group. This is important in preventing the rejection of one claim in a group from being applied against others of the claims in the group.

Applicant respectfully submits that the grounds of rejection of claims as specified below meet the requirements of 37 CFR 1.192(c)(7). However, if the Examiner disagrees, and in order to avoid an abandonment of the application, applicant will adopt, as a last resort, the grouping of the claims as proposed by the Examiner. This is to avoid the following in MPEP 1206:

"The question of whether a brief complies with the rule is a matter within the jurisdiction of the examiner."

The Examiner should understand that applicant is willing, as a last resort, to accept the grounds of rejection by the Examiner of the claims only to avoid any possibility of a holding by the Examiner that the application is abandoned for a failure by applicant to specify proper grounds of rejection claims. Applicant is confident that the Examiner will not be arbitrary in making any decision that applicant has not specified proper grounds of rejection and that the Examiner's grounds of rejection of the claims will apply.

Applicant's proposed grounds of rejection of the claims are as follows:

C. Grounds of Rejection Relating to Claim 1 and 4

Claims 1 and 4 recite a patentable combination that includes first and second electrodes wherein the first electrode is constructed, disposed and biased to ionize molecules of an inert gas and the second electrode is constructed, disposed and biased to obtain a movement of ions of the inert gas to a wafer at a low and controlled speed for an etching of the insulating layer of the wafer by the ions at the low and controlled speed. Claims 1 and 4 are patentable over Koshimizu patent 5,990,687 as demonstrated by Mountsier, and over Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these features.

D. Grounds of Rejection Relating to Claims 2, 5, 6, 9, 16, 45, 46, 47 and 50.

In addition to reciting the first and second electrodes as specified in group C, claims 2, 5, 6, 9, 16, 45, 46, 47 and 50 recite the additional features that first and

second electrical conducting members are respectively associated with the first and second electrodes to create first and second electrical fields. These additional features cause the claims in the ground D of rejection to be patentably distinguished from the claims in the ground C of rejection. These additional features, in combination with features discussed above in the ground C of rejection and recited in the claims in the ground C of rejection, cause claims 2, 5, 6, 9, 16, 45-47 and 50 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu or Mountsier discloses these additional features.

E. Grounds of Rejection of Claim 3

1. First and second sources of alternating voltage are recited in claim 3 for creating biases respectively on the first and second electrodes, the biases on the electrodes being negative direct voltages and the bias on the second electrode being less than the bias on the first electrode. These features are in addition to features recited in the claims in the grounds C and D of rejection. These additional features cause claim 3 to be patentably distinguished from features discussed above in the grounds C and D of rejection and recited in the claims in the grounds C and D. These additional features, in combination with the features discussed above in the grounds C and D, cause claim 3 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these additional features or the features specified above in the grounds C and D of rejection.

F. Grounds of Rejection of Claims 7, 21, 43 and 44

1. Claims 7, 21, 43 and 44 recite first and second sources of alternating voltage respectively to produce voltages or electrical fields of high and low magnitudes on, or in the vicinity of, the first and second electrodes for the creation respectively of first and second electrical fields of high and low strength in an enclosure. The wafer is disposed relative to the ions of an inert gas to receive an etching of a low magnitude on the surface of the insulating layer in the wafer. These features are in addition to the features recited in claims specified above in grounds C, D and E of rejection. These additional features cause claims 7, 21, 43 and 44 to be distinguished patentably over the claims in the grounds C, D and E of rejection. These additional features, in combination with the features specified above in the claims in grounds C-E, also cause claims 7, 21, 43 and 44 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these additional features or the features specified above in groups C-E.

G. Grounds of Rejection of Claim 8

1. Claim 8 recites that one of the electrodes is contiguous to, but spaced from, the wafer. These features are in addition to the features recited in the claims specified above in the grounds C-F of rejection. These additional features cause claim 8 to be distinguished patentably over the claims in the grounds C-F of rejection. These additional features, in combination with features specified above in the grounds C-F of rejection, also cause claim 8 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier

discloses these additional features or features specified above in the grounds C-F of rejection.

H. Grounds of Rejection of Claims 11, 14, 19, 48, 49 and 51

1. In claims 11, 14, 19, 48, 49 and 51, the wafer is recited as being disposed relative to one of the electrodes to create first and second capacitors, one having a low impedance and the other having a high impedance. These features are in addition to the features recited in the claims specified above in the grounds C-G of rejection. These additional features cause the claims in the ground H of rejection to be patentably distinguished from the claims in the grounds C-G of rejection. These additional features, in combination with features specified above in grounds C-G, cause claims 11, 14, 19, 48, 49 and 51 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these additional features or the features specified above in the grounds C-G of rejection.

I. Grounds of Rejection of Claims 10, 12, 17, 18 and 20.

1. Claims 10, 12, 17, 18 and 20 recite that the wafer is disposed between the first and second electrodes and a floating potential is provided on the wafer relative to the negative potential on the first and second electrodes. These features are in addition to the features recited in the claims specified above in the grounds C-H of rejection. These additional features provide a patentable distinction over the features recited in the claims in the grounds C-H of rejection. These additional features, in combination with the features specified above in the grounds C-H of rejection, also cause claims 10, 12, 17, 18 and 20 to be allowable over Koshimizu as demonstrated by

Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these additional features or the features specified above in the grounds C-H of rejection. As will be seen from the above discussion, applicant agrees with the Examiner that all of the claims 10, 12, 17, 18 and 20 should be included in the same ground of rejection.

J. Grounds of Rejection of Claim 13.

1. The wafer is recited in claim 13 as being disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure. These features are in addition to features recited in the claims specified above in the grounds C-I of rejection. These additional features cause claim 13 to be patentably distinguished from the features recited in the claims in the grounds C-I of rejection. These additional features, in combination with the features specified above in the grounds C-I of rejection , also cause claim 13 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these additional features or the features specified above in the grounds C-I of rejection.

K. Grounds of Rejection of Claim 15.

1. In claim 15, there is a recitation that the first capacitor includes a dielectric of the molecules and ions of the inert gas and the second capacitor includes a dielectric constituting the insulating layer(s) in the wafer. These features are in addition to the features recited in the claims specified above in the grounds C-J of rejection. These

additional features are patentably distinguished from the features recited in the claims in the grounds C-J of rejection. These additional features, in combination with features specified above in the grounds C-J of rejection, also cause claim 15 to be allowable over Koshimizu as demonstrated by Mountsier, and Koshimizu in view of Mountsier, because neither Koshimizu nor Mountsier discloses these additional features or the features specified above in the claims in the grounds C-J of rejection.

L. Allowability of Each Individual claim in the Grounds of Rejection with More than One (1) Claim.

Certain of the grounds of rejection include more than one (1) claim. As will be seen from the subsequent discussion, applicant believes that each claim in each of such grounds is individually allowable over the prior art cited by the Examiner. Therefore, applicant will analyze separately each claim in each ground of rejection.

VII. Argument.

A. General Discussion Relating to the Differences Between Applicant's Invention (Not Applied Specifically to any of the Claims) and the prior art cited by the Examiner.

1. Claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 have been rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu patent 5,980,687 as demonstrated by Mountsier patent 5,810,933. The Examiner has had to cite two (2) references in combination to reject these claims. The claims are accordingly not anticipated by Koshimizu even by the Examiner's reasoning.

2. Koshimizu discloses an aggregation rather than a combination.

The Examiner has applied the electrodes 116 and 110, the wafer W attached to the electrode 116 and the conduit 202 in Koshimizu against claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50. The citation of the electrodes 116 and 110 against these claims constitutes an aggregation. This results from the fact that the electrode 110 has no effect on the production of a deposition on the wafer W attached to the electrode 116. Similarly, the electrode 116 has no effect on the production of a deposition on the wafer W attached to the electrode 110. This may be seen from the following statement in Koshimizu at column 6, lines 27-30:

> "Moreover, in the etching apparatus 100, wafers W fixed on the first and second susceptors 110 and 116 can simultaneously be subjected to the same etching process, thereby increasing the throughput of the apparatus." (Underlining supplied.)

A simultaneous deposition of two (2) wafers, each deposition performed independently of the other, does not mean that the apparatus for producing the two (2) wafers constitutes a combination.

Stating the results simply, the operation of the electrode 110 in Koshimizu does not affect the deposition produced on the upper one of the wafers in Figure 3 by the voltage on the electrode 116. Similarly, the operation of the electrode 116 does not affect the deposition produced on the lower one of the wafers W in Figure 3 by the voltage on the electrode 110. Furthermore, as will be discussed in detail subsequently, Mountsier

does not teach or demonstrate what Koshimizu allegedly discloses but does not make operative.

The Examiner has admitted on page 8 of the Office Action dated October 11, 2003 that Koshimizu discloses an aggregation rather than a combination. This may be seen from the following statement by the Examiner at the top of page 8 of the Office Action:

> "The Examiner agrees that Koshimizu operates the second 110 and first electrodes 116 independently of each other to process any number of wafers including one." (Underlining supplied).

The word "independently" indicates that Koshimizu's apparatus is an aggregation.

Since the Koshimizu apparatus constitutes an aggregation, Koshimizu discloses two substantially identical combinations. One combination includes the electrode 116 (but not the electrode 110) and the wafer W closest to the electrode 116 and the other includes the electrode 110 (but not the electrode 116) and the wafer W closest to the electrode 110. As a result, Koshimizu does not disclose a combination including two (2) electrodes. There may be two (2) separate combinations in Koshimizu, but the two (2) combinations constitute an aggregation. There is accordingly only a single electrode (116 or 110) in one of the two (2) separate and independent combinations in Koshimizu and the other (116 or 110) in the other one of the two (2) separate combinations in Koshimizu.

All of applicant's claims involve a combination of two (2) electrodes. These two (2) electrodes are interrelated in a single combination. Because of this, there is a

fundamental difference between the single combination recited in applicant's claims and the two (2) independent and aggregative combinations in Koshimizu.

3. There is another fundamental difference between the single combination recited in applicant's claims and the two (2) independent and aggregative combinations in Koshimizu. One of applicant's electrodes (24) is involved in producing argon ions from argon molecules. The electrode 24 receives a high voltage. The other (22) of applicant's electrodes is involved in etching a surface 12 of an insulated layer 14 in a wafer 16 at a low and controlled voltage and at a low energy to provide a smooth surface on the layer. In contrast, the electrodes 116 and 110 in Koshimizu perform the same function. Furthermore, neither of the electrodes 116 and 110 in Koshimizu etches a surface of the wafer W at a low and controlled rate to provide the surface with a smooth configuration.

4. There is a further significant difference between applicant's invention and Koshimizu. As shown in Figures 4a and 4b of applicant's drawings, applicant provides two (2) capacitors 52 and 54 in a series relationship. One of these capacitors has a high impedance. This limits to a low value the current flowing through the capacitors. This low current causes the etching of the material on the surface 12 of the layer 14 to be smooth and uniform. Koshimizu does not disclose these features.

B. Misstatements and unsupported statements by the Examiner concerning Koshimizu and Mountsier

In the Office Action dated July 11, 2003, the Examiner has made a number of statements about the construction and operation of the Koshimizu apparatus

that are not supported by the specification and drawings in Koshimizu. These include the following:

1. According to the Examiner on page 4 of the Office Action dated July 11, 2003, a first member 104 is disposed in Koshimizu adjacent the first electrode 116 for providing a reference potential different in magnitude from the bias on the first electrode. However, Koshimizu does not disclose the magnitude of the voltage on either of the electrodes 116 and 110. Thus, the Examiner's statement about voltage is unsupported. Furthermore, Koshimizu does not disclose the distance between the electrode 116 and the container 104. However, judging from Figure 1 in Koshimizu, the electrode 116 and the container 104 do not appear to be adjacent each other. Koshimizu also does not disclose that the electrode 116 and the first member 104 produce a first electrical field.

2. The Examiner states on page 4 of the Office Action dated July 11, 2003 that the annular rail 204 is adjacent the electrode 110 for providing the reference potential to create a second electrical field. The voltage applied to the electrode 110 is not disclosed in Koshimizu. Koshimizu also does not disclose the application of any voltage to the electrode 110 or the annular rail 204. Koshimizu additionally does not disclose that the annular rail 204 is adjacent to the electrode 110. Figure 3 in Koshimizu does not indicate any such adjacent relationship. It would appear that no electrical field is created by the electrode 110 and the annular rail 204. This is particularly true since the annular rail 204 appears to be floating because it is disposed on the insulating support plate 108.

3. There is a statement by the Examiner on page 4 of the Office Action dated July 11, 2003 that a first source 134 of alternating voltage in Koshimizu

creates a bias on the electrode 116, this bias being a negative direct voltage. There is no indication in Koshimizu that the alternating voltage from the source 134 creates a bias of a negative direct voltage. The Examiner attempts to use applicant's disclosure to support the Examiner's statement that there is a bias of a negative direct voltage on the electrode 116 in Koshimizu. However, Koshimizu does not disclose the production of positive ions in first half cycles and negative electrons in the other half cycles. Therefore, applicant's disclosure is not applicable to Koshimizu.

4. The Examiner states on page 3 of the Office Action dated July 11, 2003 that the second source 130 of alternating voltage in Koshimizu creates a bias on the electrode 110, this bias being a negative direct voltage. There is no indication in Koshimizu that the alternating voltage from the source 130 creates a bias or that any such bias is a negative direct voltage.

5. The Examiner states on page 4 of the Office Action dated July 11, 2003 that "...it is anticipated by Koshimizu and common practice in the art that all wafers (or other articles) positioned on supports or electrodes would necessarily have a gap between the wafer/article and the support surface upon which the wafer/article is resting or electrically clamped." This is an unsupported statement by the Examiner. The Examiner should be required to provide support in the prior art for this statement, particularly since the Examiner states that this is "common practice in the art." If it is "common practice in the art," the Examiner should have no difficulty in providing a prior art reference that discloses that it is "common practice." Furthermore, the sentence quoted above with the

words "and where providing a direct current bias as a result of the first (134) and second (130) sources of alternating voltage" has no meaning, particularly since there is no verb.

6. The Examiner then states on pages 4 and 5 of the Office Action dated July 11, 2003:

> "This is demonstrated by Mountsier who shows a typical wafer-support interface (62/52; Figure 6). As such, when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent."

Where does Mountsier "demonstrate" this? Applicant finds no demonstration to this effect in Mountsier. Certainly the structure 62/52 in Figure 6 of Mountsier does not disclose this. Applicant would appreciate it if the Examiner would specify in the Examiner's answer where Mountsier demonstrates this. Furthermore, the structure in Mountsier does not appear to be substantially to the standard in applicant's claims. Anyhow, what is the structure in applicant's claims to which the Examine is referring?

7. According to the Examiner on page 3 of the Office Action dated July 11, 2003, "the first (116) electrode is contiguous (neighboring) to, but spaced from, the wafer (W attached to the electrode 116 Figure 1, 3)." If the wafer is attached to the electrode 116, the wafer cannot be contiguous to the electrode. Furthermore, the wafer W is not "contiguous" or "neighboring" to the electrode 116. Koshimizu indicates in column 4, lines 8-10, that the electrode 116 "can fix a wafer W thereon." This prevents the wafer W and the electrode 116 from being contiguous. Furthermore, the drawings in Koshimizu show the wafer W as being disposed on the electrode 116.

8. In column 4, lines 48-51, Koshimizu states:

> "Thus, predetermined high frequency powers are, preferably the same high frequency power is, applied to the first and second susceptors 110 and 116, respectively."

The word "preferably" in the above quotation does not indicate that Koshimizu discloses that different amounts of power are applied to the susceptors 110 and 116. Even if different amounts of power should be applied to the susceptors 110 and 116, Koshimizu does not disclose which one of the susceptors receives the greater amount of power.

9. According to the Examiner on page 6 of the Office Action dated July 11, 2003:

> "Mountsier, as stated above, teaches a wafer support platform (52, Figure 5; column 4, lines 20 23) (sic) that provide a series relationship between two capacitors, one (68 dielectric gap; Figure 5; column 4, lines 20-23) having a high capacity impedance and the other (80/82 dielectric gap; Figure 6) having a low capacity impedance. In particular, because the wafer support 52 is made of an electrical insulator (ceramic, column 5, lines 8-20) capacitance across the stated points is established and the wafer (62) is electrically floated."

This statement by the Examiner is incomprehensible to applicant. It is accordingly difficult for applicant to refute this statement.

10. Applicant respectfully disagrees with the Examiner's position that Mountsier discloses two (2) capacitors and that, if there are two (2) capacitors, one has a high impedance and the other has a low impedance. This may be seen primarily from Figures 5, 6 and 7 in Mountsier. In Figure 5, the different elements shown have the following properties:

68 - gap filled with a gas such as helium or nitrogen

52 – ceramic disk

54 – layer of thermally conductive paste

56 – metal support disc

58 – layer of thermally conductive paste

60 – metallic coating disc

Figures 5, 6 and 7 in Mountsier show a device for cooling the wafer 62. There is no discussion by Mountsier that the device provides electrical capacitors. Furthermore, the elements 54 and 58 constitute thermally conductive paste. A thermal conductor is not necessarily an electrical conductor. If the elements 54 and 58 are electrically conductive, only the ceramic disc 52 is dielectric. This prevents the device in Figures 5, 6 and 7 from providing two (2) capacitors. If the elements 54 and 58 are electrical insulators, it is possible to have two (2) capacitors in series assuming that the metal support disc 56 serves as a conductive plate in each of the capacitors. However, Mountsier does not disclose that the elements 54 and 58 are electrical insulators.

Even if Figures 5, 6 and/or 7 in Mountsier can be considered to provide two (2) capacitors, one does not have a high impedance and the other a low impedance. There is no statement in Mountsier to this effect. Furthermore, the dimensions of the elements in Figure 5 of Koshimizu do not support this. Figure 6 in Koshimizu is no help to the Examiner in this regard since Figure 6 shows only the wafer 62 and the ceramic disc 52.

Of course, it is possible that one of the thermally conductive plates 54 and 58 may be electrically conductive and the other may be electrically insulating. This further

establishes that Mountsier has not provided a sufficient disclosure to support the Examiner's position since it provides different possibilities, not clarified, in each of Koshimizu and Mountsier.

C. Differences between applicant's invention and Koshimizu (as applied specifically to the claims).

Claim 1

Claim 1 is allowable over Koshimizu because Koshimizu does not disclose a first electrode and magnetic members disposed relative to each other and to molecules of an inert gas for ionizing molecules of the inert gas. There is also disclosure in Koshimizu that a second electrode and a wafer are disposed relative to each other and to the ions of the inert gas, and the second electrode is constructed, to obtain a movement of the ions to a surface of an insulating layer in the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at the low and controlled speed. Certainly neither the electrode 110 nor the electrode 116 in Koshimizu performs this function.

Claim 2

Claim 2 is dependent from claim 1 and is accordingly allowable over Koshimizu for the same reasons as claim 1. Claim 2 is also allowable over Koshimizu because Koshimizu does not disclose that a first electrical field and a magnetic field are disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas. Koshimizu also does not disclose that a second electrical field and the magnetic field are disposed relative to each other and to the ions of the inert gas

to obtain the movement of the ions to the wafer at the low and controlled speed for an etching of the surface of the wafer by the ions at the low and controlled speed.

Claim 3

Claim 3 is allowable over Koshimizu because it is dependent from allowable claim 1. Claim 3 is also allowable over Koshimizu because it recites that the bias on the first electrode is a negative direct voltage and is created by an alternating voltage source. The same recitations are provided in claim 3 for the second electrode.

Claim 4

Claim 4 is allowable over Koshimizu because it is dependent from allowable claim 1. Claim 4 is also allowable over Koshimizu because it recites a path for the flow of argon molecules from the vicinity of the first and second electrodes and the magnetic members.

Claim 5

Claim 5 recites that the wafer is at a floating potential. Koshimizu does not disclose this.

Claim 6

Claim 6 recites that the first and second electrically conductive members are respectfully adjacent, but spaced from, the first and second electrical conductors at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

Claim 7

Koshimizu does not disclose certain of the features recited in claim 7. For example, Koshimizu does not disclose a first electrode and a first source of an alternating voltage for producing a direct negative voltage of a high magnitude on the first electrode for the creation of a first electrical field of a high magnitude in an enclosure. There is also no disclosure in Koshimizu of a second electrode and a second source of an alternating voltage for producing a direct negative voltage of a low magnitude on the second electrode for the creation of a second electrical field of a low magnitude in the enclosure. No disclosure is further provided in Koshimizu that the wafer is disposed relative to the second electrode and to the ions of the inert gas in the enclosure to receive an etching of a low magnitude on the surface of an insulating layer in the wafer by the ions of the inert gas in the enclosure.

Claim 8

Because of its dependency from claim 7, claim 8 is allowable over Koshimizu for the same reasons as claim 7. Claim 8 is also allowable over Koshimizu because of the recitation of the operation of the first and second sources of alternating voltage respectively to produce a direct voltage of a high magnitude and a negative polarity on the first electrode and to produce a direct voltage of a low magnitude and a negative polarity on the second electrode and because of the recitation that the second electrode is disposed in a contiguous, but spaced, relationship to the wafer.

Claim 9

Claim 9 recites that the first electrical conductor is disposed in adjacent relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor. A similar relationship is recited between the second conductor and the second electrical conductor. Koshimizu does not disclose these relationships.

Claim 10

Claim 10 recites that the wafer is at a floating potential relative to the negative potentials on the first and second electrodes and relative to the reference potential. Koshimizu does not disclose this relationship.

Claim 11

Claim 11 is allowable over Koshimizu because Koshimizu does not disclose that the wafer is disposed in a spaced, but adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure. Claim 11 is also allowable over Koshimizu for the same reasons as discussed above with respect to claim 7 because it is dependent from claim 7.

Claim 12

Claim 12 recites that there is a space between the second electrode and the second conductive member for the flow of the molecules and ions of the inert gas from the enclosure. Koshimizu does not disclose this.

Claim 13

Koshimizu does not disclose that the wafer is disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure. Because of this, claim 13 is allowable over Koshimizu.

Claim 14

Claim 14 is allowable over Koshimizu because Koshimizu does not disclose the following elements such as recited in the claim: (a) a first source of an alternating voltage, (b) a first electrode, (c) a second source of an alternating voltage, (d) a second electrode and (e) the recitation in lines 16-19 that the second electrode and the wafer provide a first capacitor of a high impedance and that the wafer and the ions in the enclosure provide a second capacitor of a low impedance in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

Claim 15

Because of its dependency from allowable claim 14, claim 15 is allowable over Koshimizu for the same reasons as allowable claim 14. Claim 15 additionally recites that the first capacitor includes a dielectric of the molecules and ions of the inert gas and that the second capacitor includes a dielectric constituting the insulating layers in the wafer. Koshimizu does not disclose these features.

Claim 16

Claim 16 is allowable over Koshimizu because Koshimizu does not disclose first and second electrically conductive members such as recited in the claim. Claim 16 is also allowable over Koshimizu because of its dependency from allowable claim 14.

Claim 17

Claim 17 recites that the wafer has a floating potential and is disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode and is substantially parallel to the first and second electrodes. Koshimizu does not disclose this.

Claim 18

Claim 18 recites that the conduit is disposed adjacent to, but spaced from, the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas are passed from the enclosure at a position adjacent to the second electrode.

Claims 19 and 20

Claims 19 and 20 are dependent from allowable claim 14 and are accordingly allowable over Koshimizu for the same reasons as claim 14. Claim 20 is additionally allowable over Koshimizu for the same reasons as discussed above for claims 15, 16, 17 and 18.

Claim 21

In claim 21, the following recitations distinguish patentably over Koshimizu: (a) an enclosure including first and second electrodes and negative members, (b) a first voltage source for producing a voltage of a high magnitude on the first electrode to obtain a production of a high electrical field in the enclosure, (c) a second voltage source for producing a voltage of a low magnitude on the second electrode to obtain a production of a low electrical field in the enclosure and (d) a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without the creation of any pits in the surface of the insulating layer.

Claims 43-47 and 50

Claims 43-47 and 50 are directly or indirectly dependent from claim 21. Because of this, they are allowable over Koshimizu for the same reasons as claim 21. Claims 43-47 and 50 are also allowable over Koshimizu for these additional reasons:

Claim 43

The recitation of the first and second electrodes in cooperation with the magnetic field to produce the results specified in the claim.

Claim 44

The cooperation between the first voltage source and the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode. The cooperation between the second voltage source and the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

Claim 45

First and second electrical conducting members respectively in co-operative relationships with the first and second electrodes.

Claim 46

The relative disposition between first and second electrical conducting members and the first and second electrodes.

Claim 47

The relative disposition between the first electrical conducting member and the first electrode and between the second electrical conducting member and the second electrode.

Claim 48

Claim 48 recites that the wafer and the electrodes define a series relationship between two (2) capacitors, one (1) having a high capacitor impedance and the other having a low capacitor impedance. Claim 48 additionally recites that the high capacitor impedance limits the energy providing for the

etching of the surface of the insulating layer in the wafer. Koshimizu does not disclose this.

Claim 49

Claim 49 recites that the wafer and one of the electrodes defines a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and that the high capacity impedance limits the energy providing for the etching of the insulating layer on the wafer. Koshimizu does not disclose this. Claim 49 is also allowable over Koshimizu because it is dependent from allowable claim 43.

Claim 50

The cooperative relationship between the first electrical conducting member and the first electrode and between the second electrical conducting member and the second electrode.

Clams 49 and 51

Claims 49 and 51 are allowable over Koshimizu for the following reasons.

Claim 49

Claim 49 recites that the wafer and one of the electrodes defines a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and that the high capacity impedance limits the energy providing for the etching of the insulating

layer in the wafer. Koshimizu does not disclose this. Claim 49 is also allowable over Koshimizu because it is dependent from allowable claim 47.

Claim 51

Claim 51 is dependent from claim 49 and is accordingly allowable over Koshimizu for the same reasons as claim 49. Claim 51 is also allowable over Koshimizu because it recites that the first voltage source applies an alternating voltage from the first voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and that the second voltage source applies an alternating voltage from the source to the second electrode to produce a weak negative direct voltage in the second electrode. Koshimizu also does not disclose that a first electrical conducting member is disposed in cooperative relationship with the first electrode to provide for the production of the high electrical field and that a second electrical conducting member is disposed in cooperative with the second electrode to provide for the production of the low electrical field.

D. The effect of the combination of Mountsier with Koshimizu to reject applicant's claims as anticipated by Koshimizu.

The claims are allowable over Mountsier for the same reasons as discussed above with respect to Koshimizu. The Examiner has referred to MPEP 2121.01 in indicating that Koshimizu is demonstrated by Mountsier. MPEP 2121.01 indicates that a second prior art reference may be combined with a first prior art reference when the first prior art reference does not provide an enabling disclosure. Apparently the

Examiner believes that Koshimizu's patent, by itself, does not provide an enabling disclosure. This is certainly not a factor in favor of the citation of Koshimizu against applicant's claims. The Examiner is then applying Mountsier to make the Koshimizu disclosure enabling. This is apparently what the Examiner means by the words "demonstrated by Mountsier" in the first sentence of Section 3 on page 2 of the Office Action dated July 11, 2003. However, if Koshimizu by itself does not provide an enabling disclosure, it does not anticipate applicant's claims.

One problem with respect to the Examiner's position is that the Examiner does not specify in the Office Action dated July 11, 2003 what is not enabling in Koshimizu with respect to applicant's claims 1-4, 7-9, 11, 14-16, 19-21, 43, 44, 45, 46, 47 and 50 and what Mountsier contributes to make Koshimizu enabling with respect to the discussion by the Examiner in Section 3 on pages 2-5 of the Office Action dated July 11, 2003. The only mention of Mountsier by the Examiner on pages 2-5 of the Office Action dated July 11, 2013 appears to be on page 3, line 6, and the next-to-last line on page 4 of the Office Action. These references to Mountsier are so vague that they have no meaning. Furthermore, the disc 52 and the wafer 62 in Figures 5-7 of Mountsier do not define first and second capacitors such as recited by applicant in the claims.

At any rate, claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 are allowable over Mountsier for all of the reasons specified above as to why these claims are allowable over Koshimizu. Since Mountsier is lacking the same features in applicant's claims as Koshimizu, Mountsier cannot "demonstrate" what Koshimizu does not teach.

Claims 1-4, 7-9, 11, 14-15, 19-21, 43-47 and 50 are also allowable over Mountsier for the reasons discussed above in detail.

E. The Rejection Of Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 And 51 Under 35 U.S.C. 103(A) As Being Unpatentable Over Koshimizu In View Of Mountsier.

Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu in view of Mountsier. All of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 are dependent from claims allowable over Koshimizu as individually specified above and are accordingly allowable over the combination of Koshimizu and Mountsier for the same reasons as specified above for the claims from which they are dependent.

1. The rejection of claims 5, 6, 13, 20 and 51

Claims 5, 6, 13, 20 and 51 also include a recitation of first and second electrical conducting members. Neither Koshimizu nor Mountsier discloses these electrical conducting members. This is another reason why claims 5, 6, 13, 20 and 51 are allowable over the combination of Koshimizu and Mountsier.

2. The rejection of claims 48 and 49

Claims 48 and 49 recite a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer. Neither Koshimizu nor Mountsier discloses two (2) capacitors having characteristics such as recited in claims 48 and 49. Contrary to the position of the Examiner, Mountsier does not teach two (2)

capacitors in a series relationship, one capacitor having a high capacitor impedance and the other capacitor having a low capacitor impedance. The structure shown in Figures 5 and 6 of Mountsier does not provide two (2) capacitors in series, one with a high capacitor impedance and the other with a low capacitor impedance. Furthermore, the structure shown in Figures 5 and 6 of Mountsier is for cooling and not for providing electrical capacitances. For example, Mountsier does not disclose whether layers 54 and 52 of thermally conductive paste are made from an electrically dielectric material or an electrically conductive material.

Furthermore, the recitation that the high capacitor impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer constitutes a structural limitation, not a functional limitation. Neither Koshimizu nor Mountsier discloses this structural limitation.

Koshimizu states the following in column 4, lines 48 and 49:

> ". . . Thus, predetermined high frequency powers are, preferably the same high frequency power is, applied to the first and second susceptors 110 and 116, respectively."

Applicant agrees with the Examiner that Koshimizu infers by the word "preferably" that one of the electrodes 110 and 116 can receive a different amount of power than the other electrode. But there is no indication of which one of the electrodes can receive the greater amount of power. There is also no disclosure in Koshimizu of the difference in the amount of power applied to the two (2) electrodes.

Applicant is not certain what the Examiner means by the word "demonstrated" on page 3, line 6 of the Office Action dated July 11, 2003. Apparently, the Examiner is not

satisfied with Koshimizu as a single reference. Since the Examiner has had to cite Mountsier in combination with Koshimizu, the claims should not be considered as anticipated by Koshimizu. Rather, the claims should be considered as patentable over the combination of Koshimizu and Mountsier since Koshimizu does not disclose a number of the features recited by applicant in the claims and Mountsier does not disclose the same features that Koshimizu fails to disclose.

F. The effect of the combination of Mountsier and applicant's alleged admission on page 12, lines 1-9 of applicant's specification to reject the claims.

Applicant has indicated above in detail all of the failures of Mountsier to disclose specific features recited in applicant's claims. As will be seen, these failures are many. These same features apply equally as well to applicant's alleged admissions on page 12, lines 1-9 of applicant's specification. The differences between applicant's invention as disclosed and claimed in this application and applicant's alleged admission on page 12, lines 1-9 of applicant's specification constitute the differences between success and failure. Applicant's prior embodiment did not provide a smooth and even etching of a surface of an insulating layer in a wafer. Applicant's apparatus as disclosed and claimed in this application provides a smooth and even etching of a surface of an insulating layer in a wafer.

G. The desirability of the submission by the Examiner of claims charts in representative claims

If applicant has not been able to persuade the Examiner from the discussion in this Fourth Supplemental Appeal Brief that Koshimizu discloses an

aggregation and that applicant's claims distinguish patentably over Koshimizu as demonstrated by Mountsier and Koshimizu in view of Mountsier, applicant would appreciate it if the Examiner would specify each of the elements in Koshimizu and Mountsier corresponding to each of the elements recited by applicant in representative claims. A claims chart separately specifying in one column each of the elements recited in applicant's representative claims and specifying in another column each of the corresponding elements in Koshimizu and/or Mountsier would perhaps be appropriate. Applicant suggests a claim chart since, in applicant's opinion, the Koshimizu and Mountsier disclosures are removed from applicant's invention and the Examiner has not applied these references on an element-by-element basis against applicant's claims to show the relationship between the elements recited in applicant's claims and the corresponding elements in each of Koshimizu and Mountsier.

H. The law relating to the combination of Koshimizu and Mountsier, and the combination of Mountsier and applicant's alleged admission, to reject the claims.

In order for different prior art references to be combined to reject a claim, the references have to disclose or suggest the combination recited in the claim. ACS Hospitality Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984). As the Federal Circuit indicated in the ACS case at 732 F.2d 1572, 1579, 221 USPQ 929, 933:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. Under Section 103, teaching of references can

be combined only if there is some suggestion or incentive to do so."

See also In re Fine, 837 F.2d 1071, 5 USPQ 2d 1596, (Fed. Cir. 1988) and In re Jones, 1958 F.2d 347, 21 USPQ 2d 1941 (Fed. Cir. 1992) in support of the holding in the ACS case.

Neither Koshimizu nor Mountsier cited by the Examiner to reject the claims in this application discloses or suggests certain of the features recited in the claims, these certain features being the same for Koshimizu and for Mountsier. Furthermore, neither Mountsier nor applicant's alleged admissions discloses or suggests certain of the features recited in the claims, these certain features being the same for Mountsier as for applicant's alleged admission. The references cannot accordingly be combined to reject the claims, these certain features being the same for Koshimizu as for Mountsier and the same for applicant's alleged admissions as for Mountsier.

I. The matter relating to the possibility of the imposition of additional fees.

Applicant mailed an appeal brief to the USPTO on November 7, 2003. This mailing was timely. Therefore, applicant respectfully submits that he should not have to pay an additional fee in filing this fourth supplemental appeal brief. However, if applicant should be required to pay an additional fee, please charge the additional fee to Account No. 06-2425.

J. Conclusion.

Reconsideration and allowance of the application are respectfully requested for all of the reasons discussed above in detail.

VIII. Appendix.

Claims on Appeal:

1. In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

a conduit for molecules of an inert gas,

a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer and further spaced from the wafer than the first electrode,

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

2. In a combination as set forth in claim 1,

a first member disposed adjacent the first electrode for providing a reference potential different from the bias on the first electrode to create a first electrical field, and

a second member disposed adjacent the second electrode for providing the reference potential to create a second electrical field,

the first electrical field and the magnetic field being disposed relative to each other and to the molecules of the inert gas from the supply for ionizing the molecules of the inert gas,

the second electrical field and the magnetic field being disposed relative to each other and to the ions of the inert gas to obtain the movement of the ions to the wafer at the low and controlled speed,

the second electrode being contiguous to, but spaced from, the wafer.

3. In a combination as set forth in claim 1,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the bias on the first electrode being less than the bias on the second electrode.

8. In a combination as set forth in claim 7,

an opening in the enclosure for the flow of the molecules and ions of the inert gas from the enclosure,

the first source of the alternating voltage being operative to produce a direct voltage of the high magnitude and a negative polarity at the first electrode,

the second source of the alternating voltage being operative to produce a direct voltage of the low magnitude and a negative polarity at the second electrode,

the first electrode being disposed in contiguous, but spaced, relationship to the wafer.

13. In a combination as set forth in claim 10,

a first electrical conductor disposed in an adjacent, but spaced, relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor,

a second electrical conductor disposed in an adjacent, but spaced, relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second conductor,

the wafer being disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

15. In a combination as set forth in claim 14,

the first capacitor including a dielectric of the molecules and ions of the inert gas and the second capacitor including a dielectric constituting the insulating layer.

16. In a combination as set forth in claim 14,

a first electrically conductive member disposed in an adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member, and

a second electrically conductive member disposed in an adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member.

21. In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure

first and second electrodes disposed in the enclosure and displaced from each other and from the wafer for producing electrical fields in the enclosure, and

magnetic members disposed in the enclosure for producing a magnetic field in the enclosure in a direction transverse to the electrical field,

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

25. A method as set forth in claim 22 wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak electrical field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the capacitor and a circuit including the capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

26. A method as set forth in claim 22 wherein

the capacitor constitutes a first capacitor and wherein

the relatively weak electrical field is defined by the first capacitor and a second capacitor in a series circuit and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and in which the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the first capacitor and to provide the first capacitor with the high impedance and wherein

a second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide the second capacitor with a relatively low impedance in comparison to the high impedance of the first capacitor.

28. A method as set forth in claim 26 wherein

the wafer is disposed in the relatively weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially through positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions and wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the first capacitor and a circuit including the second capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

29. A method as set forth in claim 26 wherein

the capacitor constitutes a first capacitor and wherein

the first capacitor and a second capacitor are in series and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and wherein

the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the capacitor and to provide the high impedance and wherein

the second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide a relatively low impedance in comparison to the high impedance of the first capacitor and wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low negative bias on the second electrode.

42. A method as set forth in claim 37 including the steps of:

introducing an alternating voltage of a first particular magnitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

introducing an alternating voltage of a second particular magnitude less than the first particular magnitude to the second electrode to produce a weak negative DC bias on the second electrode for the creation of the weak electrical field, and

providing a high impedance between the second electrode and the wafer and a low impedance between the wafer and the charged particles near the wafer to produce a transfer of charged particles with limited energy to the surface of the insulating layer and the walls of the socket in the insulating layer and to provide the weak and controlled etching of the surface of the insulating layer and the walls of the socket with a substantially uniform thickness of material from the insulating layer and the wall of the socket without pitting the surface of the insulating layer or the walls of the socket.

43. In a combination as set forth in claim 21 wherein,

the first electrode provides the high electrical field in cooperation with the magnetic field for producing an ionization of molecules of the inert gas in the enclosure and wherein

the second electrode provides the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer.

44. In a combination as set forth in claim 21 wherein

the first voltage source applies an alternating voltage from the voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

45. In a combination as set forth in claim 21 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

46. In a combination as set forth in claim 45 wherein

the first and second electrodes are substantially parallel to the wafer and wherein

the first and second electrical conducting members are substantially parallel to the first and second electrodes.

49. In a combination as set forth in claim 47 wherein

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

50. In a combination a set forth in claim 44 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

51. In a combination as set forth in claim 49 wherein

the first voltage source applies an alternating voltage from the first voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode and wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the strong electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the weak electrical field.

The Commissioner is authorized to credit any overpayment or charge any additional fees in this matter to our Deposit Account No. 06-2425. A duplicate of this paper is enclosed.

Respectfully submitted,

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